REMARKS

Claims 1-51 are pending in the present application. Claims 1, 23, 34, 45-47, and 49-51 are amended above. Claims 12-22 and 48 are canceled above. No new matter is added by the claim amendments. Entry is respectfully requested.

Claims 1-4, 6-11, 13-15, 17, 26, 27, 29, 31-42, 44-47, 50 and 51 are rejected as being unpatentable over Halbert, *et al.* (U.S. Patent No. 6,625,687) in view of Gustavson (U.S. Patent No. 6,442,644), Dodd (U.S. Patent No. 6,530,006), Hansen (U.S. Patent No. 5,742,840) and the Applicant's admitted prior art (AAPA). Claims 5, 16 and 28 are rejected as being unpatentable over Halbert, *et al.* in view of Gustavson, Dodd , Hansen, AAPA, and Johnson, *et al.* (U.S. Patent No. 5,987,576). Claims 12, 18-22 and 48 are rejected as being unpatentable over Halbert, *et al.* in view of Gustavson, Hansen and AAPA. Claims 23 and 49 are rejected as being unpatentable over Halbert, *et al.* in view of Dodd. Claims 24, 25, 30 and 43 are rejected as being unpatentable over Halbert, *et al.* in view of Dodd, Hansen and AAPA. Reconsideration and removal of the rejections are respectfully requested.

Independent claims 1 and 47 are amended above to state that the "memory write clock signal" has "substantially the same propagation delay" as the "data" that are "transferred from the second buffer to the memory device" and to state that the "memory read clock signal" has "substantially the same propagation delay" as the "data" that are "transferred from the memory device to the second buffer".

Independent claims 23 and 49 are amended above to state that the "memory write clock signal" has "substantially the same propagation delay" as the "data" that are "transferred from the buffer to the memory device".

Independent claims 34 and 50 are amended above to state that the "memory read clock signal" has "substantially the same propagation delay" as the "data" that are "transferred from the memory device to the buffer".

Independent claims 45 and 46 are amended above to state that the "memory write clock signal" has "substantially the same propagation delay" as the "data" that are "transferred from the buffer to the memory device" and to state that the "memory read clock signal" has "substantially the same propagation delay" as the "data" that are "transferred from the memory device to the buffer".

As stated in the specification as filed at page 10, lines 22-27, in one exemplary embodiment of the present invention:

> The module write clock signal WCLK_MDL line and the module read clock signal line RCLK_MDL are preferably routed with the data bus lines DQ on the memory module between the data buffer 48 and the memory device 44 such that the clock signals WCLK_MDL, RCLK_MDL and the data signals DQ experience the same propagation delay. In this manner, the transmitted data and clock signals will arrive simultaneously at the receiving unit, and therefore the received clock signal can be used to clock the data signals with precision.

In this manner, the memory write clock signal (for example signal WCLK_MDL of FIG. 3) that is generated by the buffer (for example DQ BUFFER 48) and transmitted to the memory device (for example DRAM device 44 of FIG. 3) experiences the same propagation delay between the buffer 48 and the memory device 44 as the corresponding data DQ to be written to the memory device. Also, the memory read clock signal (for example signal RCLK_MDL) that is returned by the memory device (for example DRAM device 44) to the buffer (for example DQ BUFFER 48) experiences the same propagation delay between the memory device 44 and the buffer 48 as the corresponding data DQ being read from the memory device.

It is respectfully submitted that none of the cited references, whether alone, or in combination, teaches or suggests the present invention as claimed. In particular, the references fail to teach or suggest the feature of "the memory write clock signal having substantially the same propagation delay as data transferred from the ... buffer to the memory device" as claimed in amended independent claims 1, 23, 45, 46, 47, and 49. In addition, the references fail to teach

or suggest the feature of "the memory read clock signal having substantially the same propagation delay as data transferred from the memory device to the ... buffer" as claimed in amended independent claims 1, 34, 45, 46, 47, and 50.

Accordingly, reconsideration of the rejections and allowance of independent claims 1, 23, 34, 45, 46, 47, 49 and 50 are respectfully requested.

With regard to the rejection of independent claims 41 and 51, it is submitted that the combination of Halbert, Gustavson, Dodd, Hansen and AAPA fails to teach or suggest the present invention as claimed. In particular, the combination fails to teach or suggest receiving a "first write clock signal ... in a first direction of transmission", receiving a "first read clock signal in a second direction of transmission", and "generating a second read clock signal in response to, and in phase with, the first write clock signal". None of the references teaches or suggests generating a "read clock signal" that is used for transmitting data in a "second direction of transmission", "in response to, and in phase with" a "write clock signal" that is used for transmitting data in a "first direction of transmission". While the Halbert reference arguably shows the transfer of data between modules in both first and second directions, Halbert does not teach or suggest correlating the read clock signal (propagating in the second direction) and the write clock signal (propagating in the first direction) in the manner claimed. Nor do any of the cited references suggest such a correlation. It is therefore submitted that the combination fails to teach or suggest the present invention as claimed.

Accordingly, reconsideration of the rejection and allowance of independent claims 41 and 51 are respectfully requested.

With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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